C8051F064

25 MIPS, 64 kB Flash, 16-Bit ADC, 100-Pin Mixed-Signal MCU

Analog Peripherals

Two 16-Bit ADCs

- ±0.75 LSB INL; no missing codes
- Programmable throughput up to 1 Msps (each ADC)
- 1 external input each; programmable as two single-ended or one differential ADC
- DMA to XRAM or external memory interface
- Data-dependent windowed interrupt generator

Three Comparators

- 16 programmable hysteresis values
- Configurable to generate interrupts or reset

Internal Voltage Reference

Precision V_{DD} Monitor/Brown-out Detector

On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler

Memory

- 4352 bytes data RAM
- 64 kB Flash; in-system programmable in 1024-byte sectors (1024 bytes are reserved)
- External parallel data memory interface

Digital Peripherals

- 59 port I/O; all are 5 V tolerant
- Hardware SMBus™ (I2C™ compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with six capture/compare modules
- 5 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset
- Real-time clock mode using timers or PCA

Clock Sources

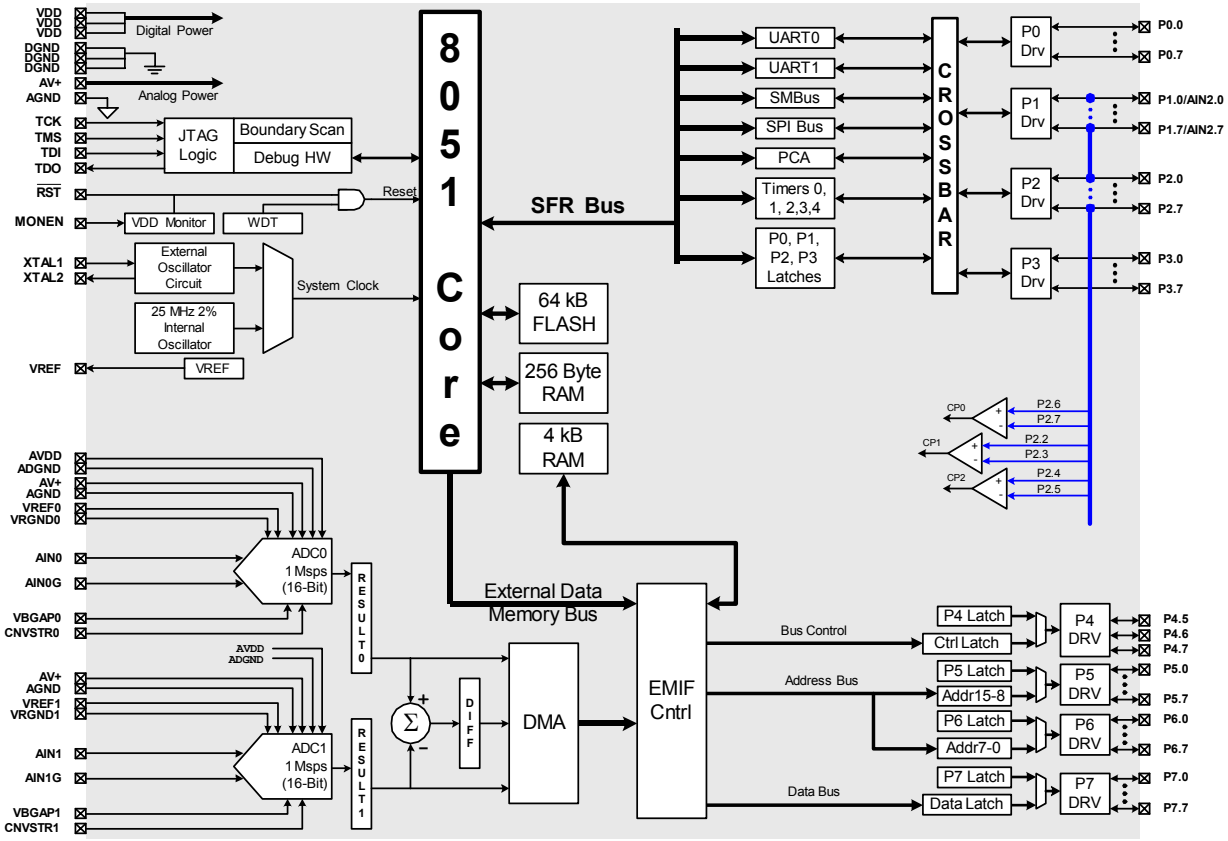
- Internal oscillator: 24.5 MHz, 2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

Supply Voltage: 2.7 to 3.6 V

- Typical operating current: 18 mA at 25 MHz
- Multiple power saving sleep and shutdown modes

100-Pin TQFP

Temperature Range: –40 to +85 °C

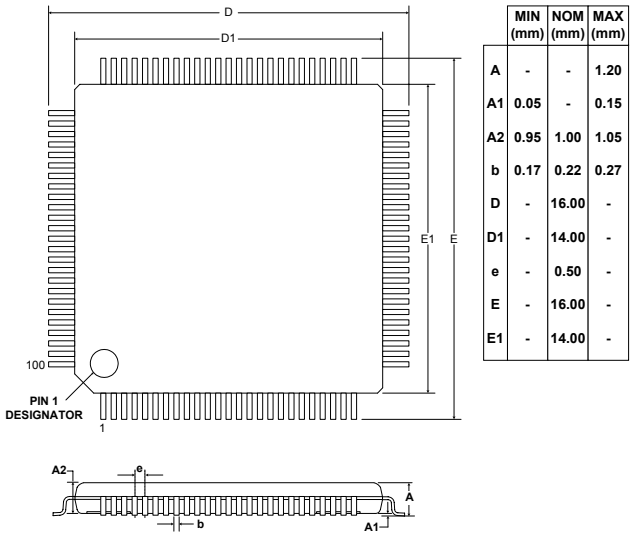


Selected Electrical Specifications

(T_A = –40 to +85 C°, V_{DD} = 2.7 V unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL CHARACTERISTICS					
Supply Voltage		2.7		3.6	V
Supply Current (CPU active)	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz; V_{DD} Monitor Enabled		18 0.7 20		mA mA µA
Supply Current (shutdown)	Oscillator not running; V_{DD} Monitor Disabled		0.1		µA
Clock Frequency Range		DC		25	MHz
16-BIT A/D CONVERTERS					
Resolution			16		bits
Integral Nonlinearity	Single-ended Mode Differential Mode		±0.75 ±0.50	±2 ±1	LSB LSB
Differential Nonlinearity	Guaranteed Monotonic		±0.5	±1	LSB
Signal-to-Noise Plus Distortion	Fin = 10 kHz, Single-ended Fin = 10 kHz, Differential		86 89		dB dB
Total Harmonic Distortion	Fin = 10 kHz, Single-ended Fin = 10 kHz, Differential		96 103		dB dB
Spurious-Free Dynamic Range	Fin = 10 kHz, Single-ended Fin = 10 kHz, Differential		97 104		dB dB
Throughput Rate				1	Msps
Input Voltage Range	Single-ended (AINn–AINnG) Differential (AIN0–AIN1)	0 $–V_{REF}$		V_{REF} V_{REF}	V V
Power Supply Current (each ADC)	Operating Mode, 1 Msps (AVDD + AV+) Shutdown Mode		5.5 1		mA µA

Package Information



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	16.00	-
D1	-	14.00	-
e	-	0.50	-
E	-	16.00	-
E1	-	14.00	-

C8051F060DK Development Kit